Amendments to the Claims

1. (*Currently Amended*) A down converter, comprising:

an integrated circuit having a control Field Effect Transistor (FET) ~~FET~~ (CF) and a synchronous rectifier FET (SF), wherein the control FET is a Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS), ~~an LDMOS FET,~~ and a conductivity-type of the LDMOS FET and a conductivity-type of a substrate are of the same type.

2. (*Currently Amended*) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a Vertical Double-Diffused Metal Oxide Semiconductor (VDMOS) ~~VDMOS~~ FET.

3. (*Original*) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a vertical trench DMOS FET.

4. (*Currently Amended*) A down converter as recited in claim 1, wherein the synchronous rectifier FET is another Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) ~~LDMOS~~ FET.

5. (*Original*) A down converter as recited in claim 2, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

6. (*Original*) A down converter as recited in claim 3, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

7. (*Original*) A down converter as recited in claim 4, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of

a few milli-Ohms from a source of the control FET and a drain of the synchronous rectifier FET to an output on a surface of a substrate.

8. (*Original*) A down converter as recited in claim 2, wherein the VDMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

9. (*Original*) A down converter as recited in claim 3, wherein the vertical trench DMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

10. (*Original*) A down converter as recited in claim 1, wherein the integrated circuit does not include isolation regions between the CF and the SF.

11. (*Original*) A down converter as recited in claim 1, wherein the conductivity type is n-type.

12. (*Original*) A down converter, comprising an integrated circuit having a control FET (CF) and a synchronous rectifier FET (SF), wherein the control FET and the synchronous rectifier FET are each LDMOS FETs, and a conductivity-type of the LDMOS FETs and a conductivity of the substrate are of the same conductivity type.

Claims 13-20 (*Cancelled*)